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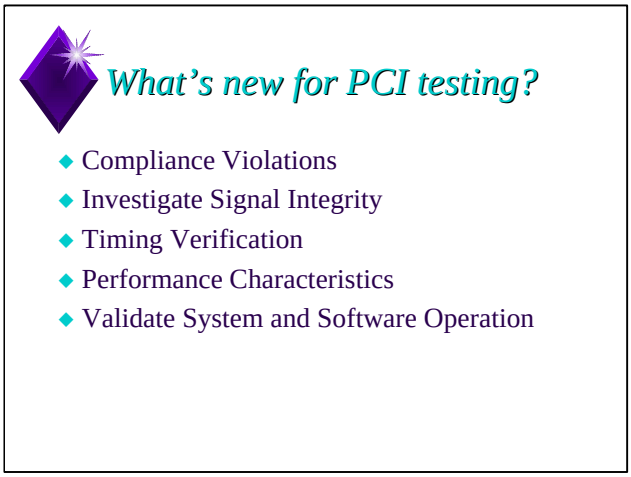
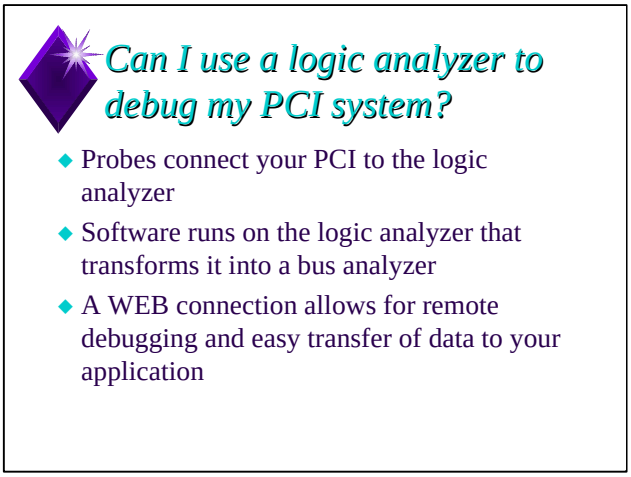
Current Activities

Vice President of FuturePlus Systems Corporation. As an electrical engineer I am involved in both the hardware and software design of many of our products.

Author Background

BSEE and MSEE in Electrical Engineering. My main area of expertise is bus architectures, both I/O and multiprocessing. This has been the focus of my career for the past eleven years. FuturePlus Systems has been involved with PCI since 1993 and is a member of the PCI Special Interest Group. Our bus analysis products are used world-wide and all our products carry Hewlett-Packard part numbers. In addition to PCI, we havebus analysis products for: USB, ISA,AGP, RAMBUS, DIMM, SIMM, VME, VME64, IEEE 1394A and FIBRE CHANNEL.





Yes you can! With products from FuturePlus Systems and Hewlett-Packard Company.

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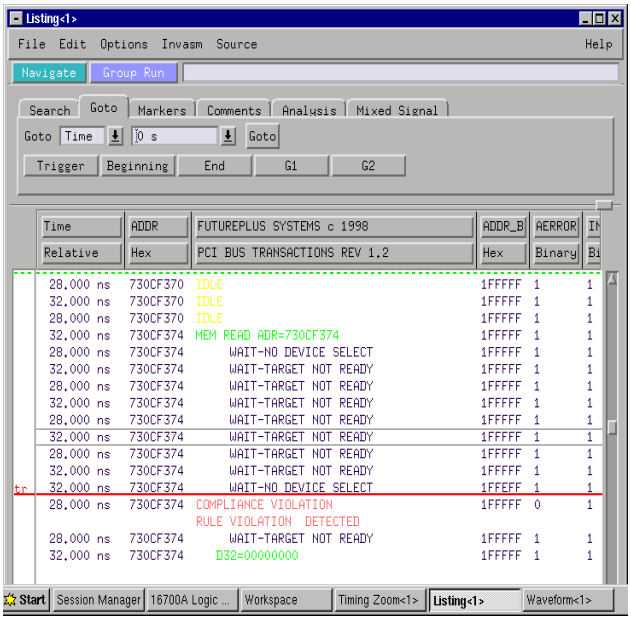
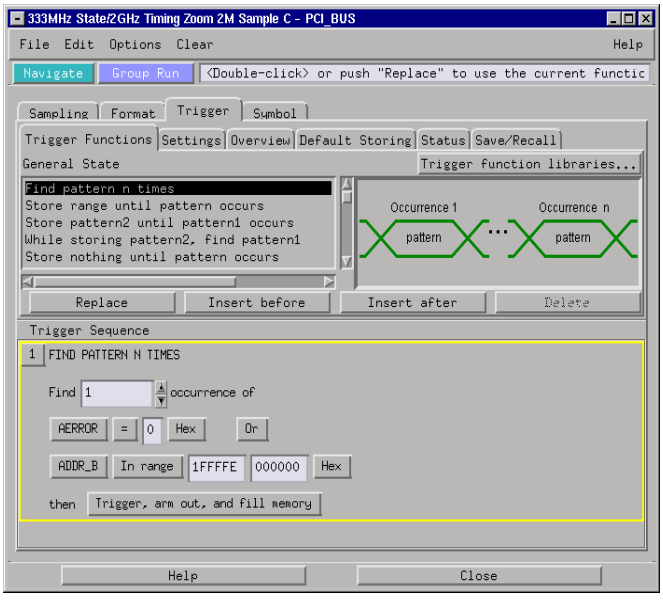
Compliance Violations



Compliance violation triggering is available on many PCI test tools today. The key to making this feature useful is to be able to quickly determine the cause of a violation.

Compliance Violation Triggering

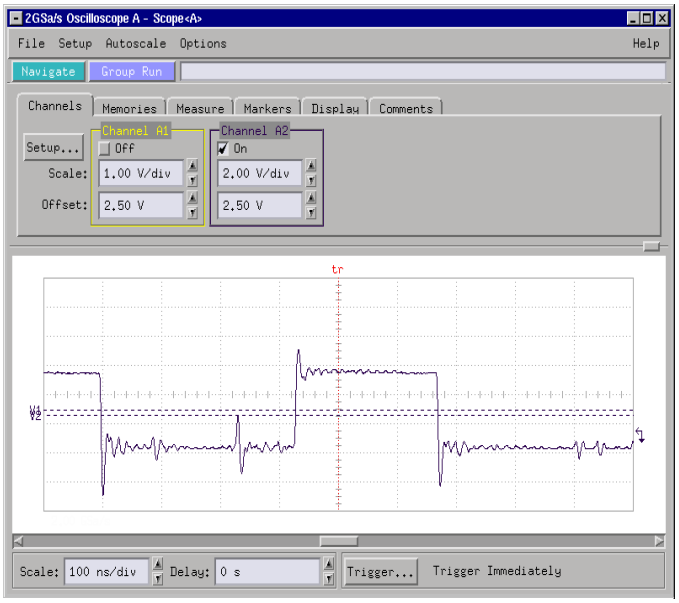


If a tool tells you a violation has occurred, that is good, but being able to trigger on a violation and see it is better. A mask to filter out known violations can also help to characterize the design you are debugging. What if a violation does occur? How do you dig deeper to find the root cause of the problem? In the trace on the previous slide we saw an illegal deassertion of DEVSEL#. Is this a chip problem? A board problem? A timing problem? A software problem? A backplane issue? A routing problem?

How many times have engineers said. "If I could find it …I could fix it…but the problem is I can't find it!" OR " I spend 90% time looking for the problem and only 10% of my time fixing it."

With a logic analysis system you can quickly track the problem down and solve it.

Signal Integrity

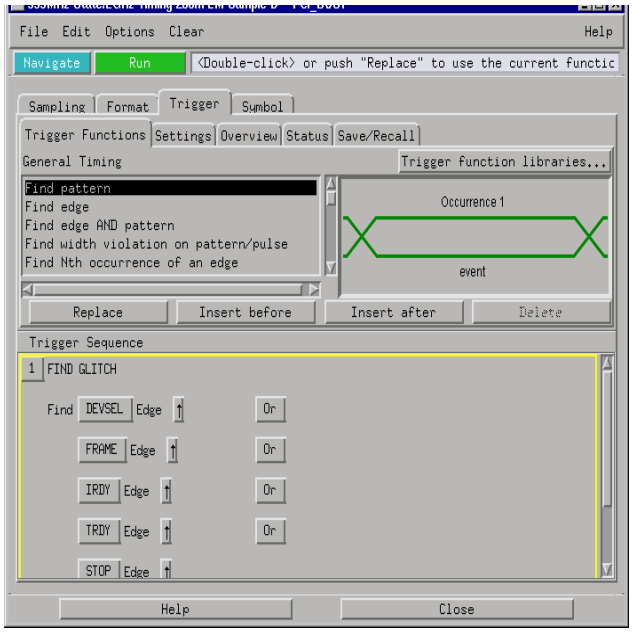


Cross-domain analysis is being able to go from the the state per clock or state per transaction domain to the timing domain and to the analog domain. Here we can actually see the glitch on DEVSEL#. Not what you expected I bet.

Chapter 4 of the PCI Specification covers the electrical environment for PCI. Signal Integrity investigation is most important in high volume applications where variation in parts, connectors, capacitors and resistors can cause failures. These types of failures sometimes show up in manufacturing but in some cases show up in the field when the user tries to install his new PCI board in his existing PCI based system. As all high volume consumer manufacturers know, failures in the field are the most expensive to fix. Costs for customer service, support and field replacement of boards can be astronomical. In addition, a company's reputation for quality can be severely tarnished.

For PCI, a robust signal integrity analysis of the design is a cost effective step in the overall design and verification process.

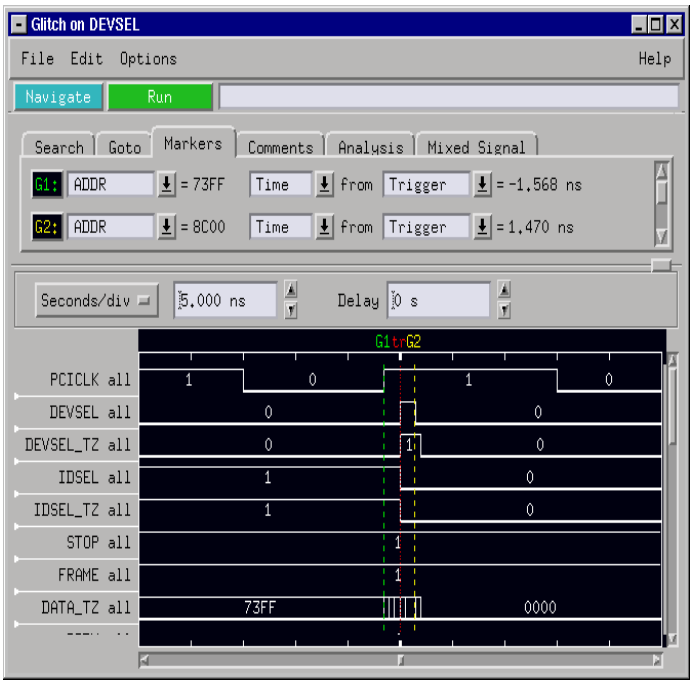
Timing Analysis



Setup and hold violation triggering can also be done by a logic analysis system. However, let's take that one step further with glitch detection. Glitches from misaligned state machines, bus contention, timing problems or signal integrity issues can be missed if your only looking for setup and hold violations. What if the problem does not occur near a rising clock edge? Does that mean it is not a problem? Glitches can propagate through logic and cause errors.

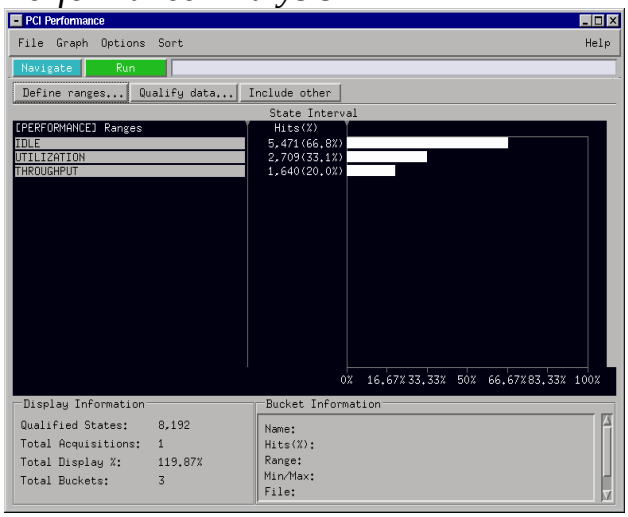
The new HP 16715A, 16716A, and 16717A modules from HP allow for glitch detection on any signal and then a 2Gs/s Timing Zoom to see the problem up close.

Glitch Detection



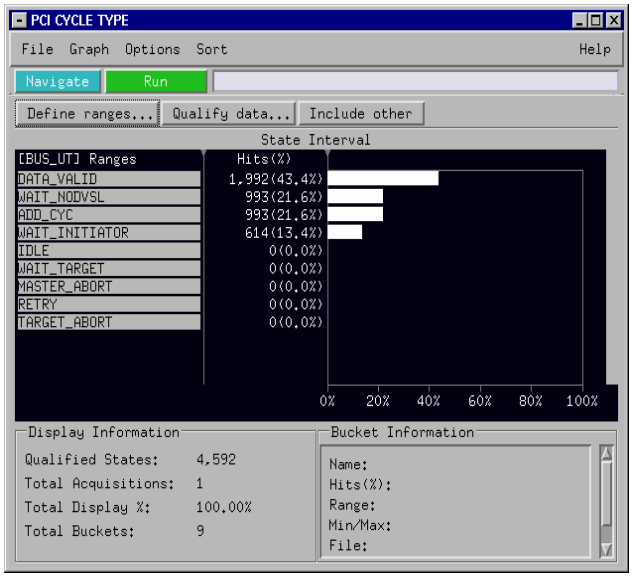
Here is that glitch on DEVSEL#. As you can see it is after the rising edge of the PCI clock. Technically not a hold violation (the spec says 0ns hold). However if the system had a 2ns clock skew, allowable by the spec, this could be a problem elsewhere on the board, inside a chip or elsewhere in the system.

Performance Analysis



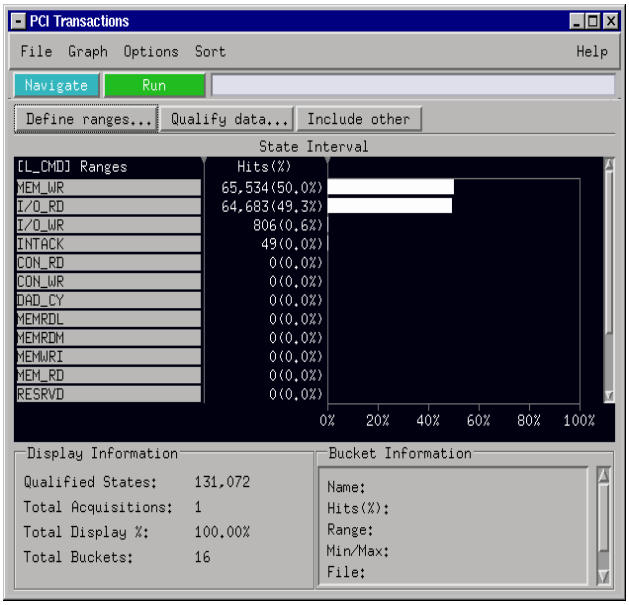
Most all PCI tools today can give you Bus Utilization, Throughput and Efficiency as you can see here. But what if you don't like what you see? Can you dig deeper to see where the problem lies? Can you find the area of your design or system where improvements can be made?

Bus Utilization : a more detailed picture



With a logic analysis system you can! A cycle by cycle breakdown of Bus Utilization can quickly help you characterize your design or that new add-in card you just added to the system. You can take this view one step further and dig even deeper. You can qualify this type of a display to show only the Bus Utilization of a certain bus master or by accesses to certain address ranges or even further qualify it by transaction type (Memory Writes for example).

Throughput: a more detailed picture



Throughput is a measurement of what percentage of the time data is actually being transferred over the bus. But how is it being transferred? What transactions are being used? What bus master is responsible for which percentage of the throughput?
These questions can all be answered by using your logic analysis system.

System Analysis

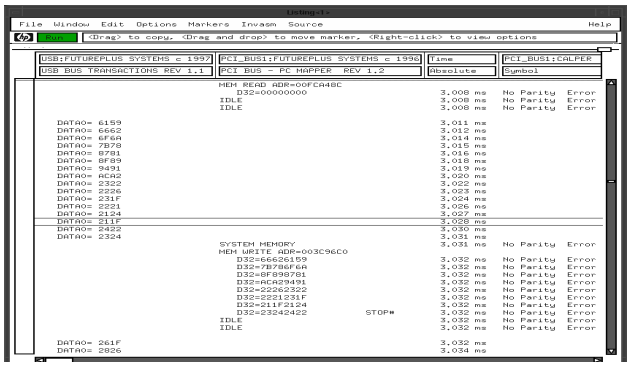
- Cross Domain Analysis
- Cross Bus Analysis
- Source Code to Signal

PCI has has come along way since 1993. At the first Compliance Workshop folks were just happy that the data got transferred correctly. Now entire systems depend on the reliability and performance of the PCI bus. Most PCI based systems today have several PCI buses or PCI buses connected to other I/O and memory buses. How do you validate the entire system? Your logic analysis system has the capability to do just that.

First let's discuss Cross Domain Analysis. That is what we saw earlier. This helps determine if we have a simple logic bug, a timing problem or an analog signal integrity problem. Cross Bus analysis is what we will look at next. This helps us track the data as it goes from bus to bus through the system.

The last area we will touch on is tracking the source code that is running on the system right down to the PCI bus.

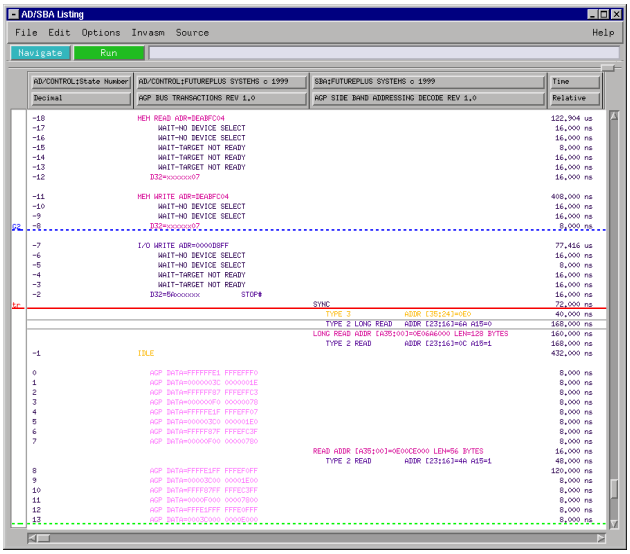
PCI to USB



Here is how we can track data from the PCI bus out onto the USB.

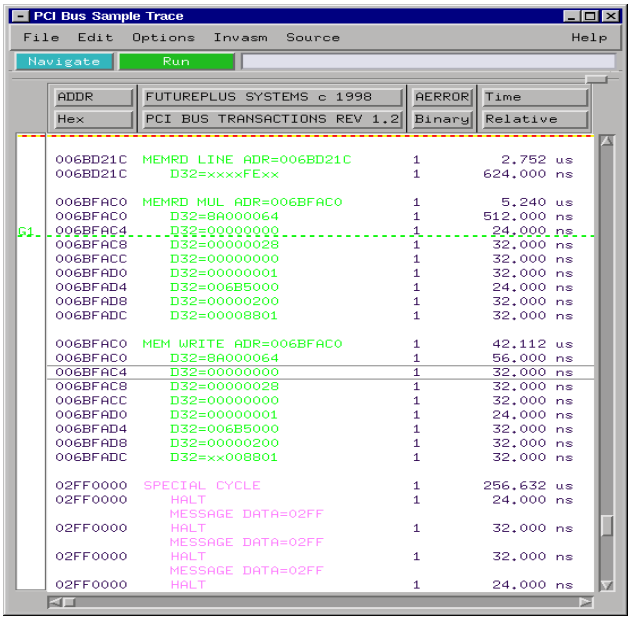
This state listing shows USB isochronous traffic from a USB Camera through the host chip set and onto the PCI. Note that the PCI bridge asserts stop after 32 bytes and the USB has 64 bytes to transfer.

AGP4X



For those of you involved in graphics design you will recognize this technology. The AGP specification was based on PCI and PCI traffic can be seen here. The AGP4X data is shown in purple and the Side Band Addressing bus is cross-bus correlated in real-time to the AGP bus so that accurate addressing information can be seen.

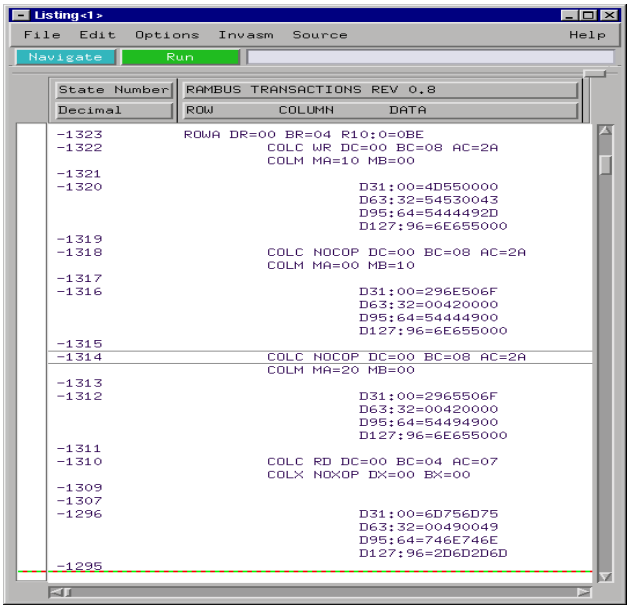
State Analysis at 66Mhz



High end PCI system analysis can greatly benefit from a logic analysis system. PCI at 66Mhz can be accurately characterized and debugged with the new HP 16715A, 16716A, and 16717A modules from HP with the 2GHz Timing Zoom.

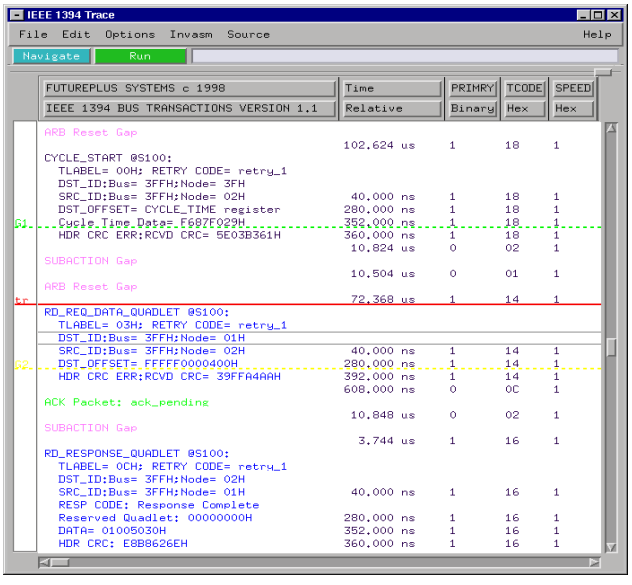
What happens if you want to trigger on a specific address but sometimes that address falls within a burst? Because of system retries and position independent code you don't know where in the burst that address occurs. You can try to add code to print out key data patterns and trigger on those as I used to do (my favorite data pattern was FEEDFACE) or you can use some of the newer PCI debug tools that increment the address during a burst to the logic analyzer.

RAMBUS



Tracking data to and from memory? Only a properly designed logic analysis system can handle the 400Mhz RAMBUS technology.

IEEE 1394A



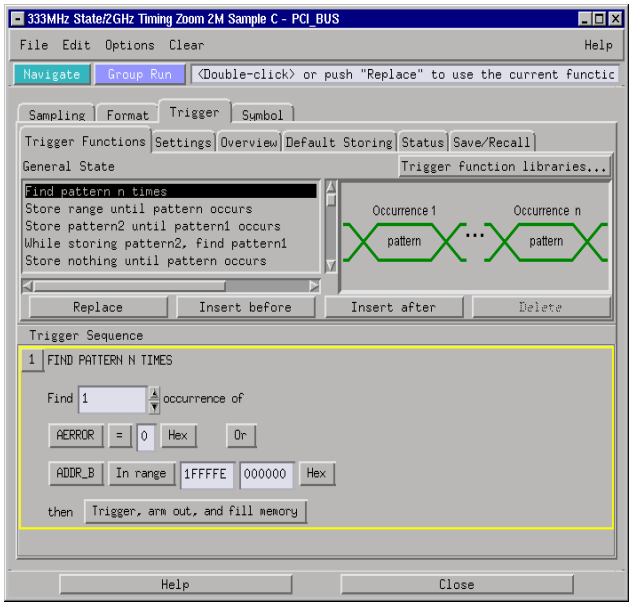
Using PCI to connect to IEEE 1394A? No problem! A logic analysis system can handle the job.

Software Testing

- Source Code to Execution
- Execution to Bus transaction
- Performance Monitoring
- Feature Filled triggering
- Deep Memory
- Post Processing tools
- WEB accessible

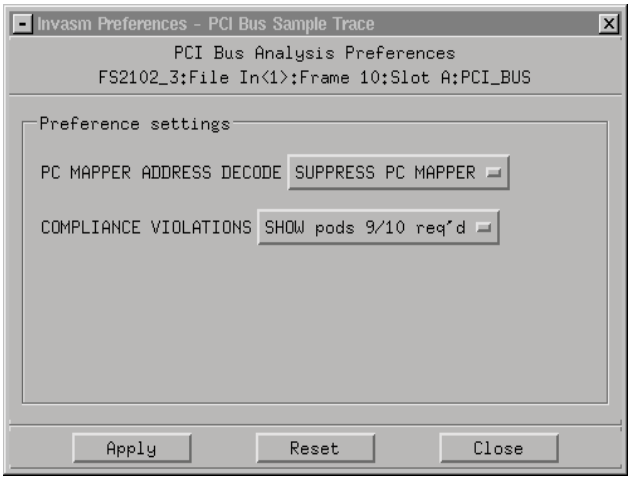
Can a software engineer benefit from a logic analysis system? The “hardware only” glass ceiling has been broken! Manufacturers of logic analysis systems are greatly motivated to serve the needs of the software engineer…and why? Software engineers now outnumber hardware engineers.

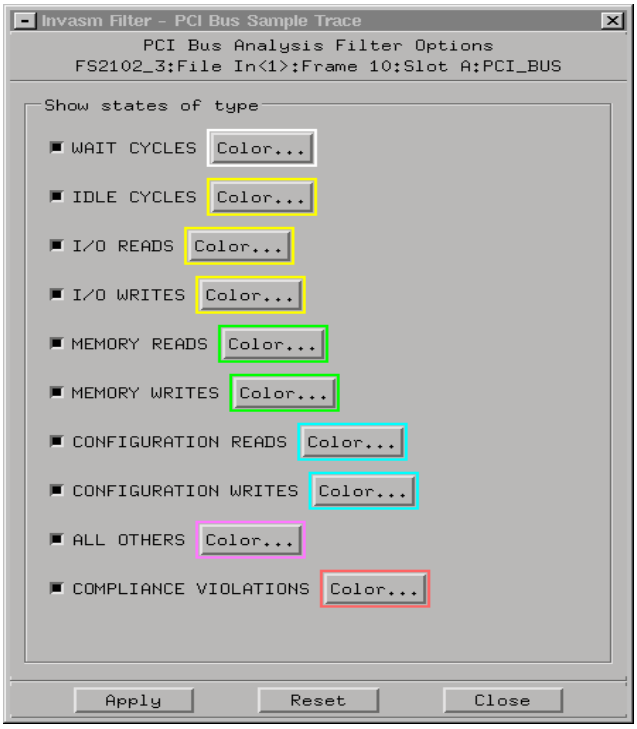
Full featured triggering



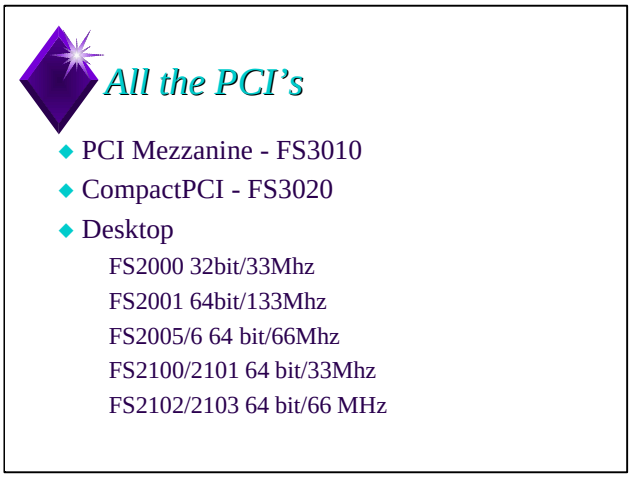
Triggering now includes
16 level sequencer
4-way branching
2 global counters
2 global timers
1 level counter
16 patterns
If-Then -Else Branching
Triggers store and recall
Pre-stored trigger macros

PCI Post Processing

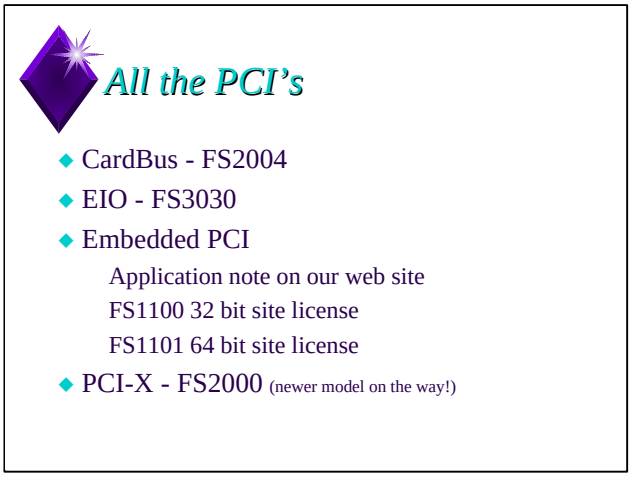




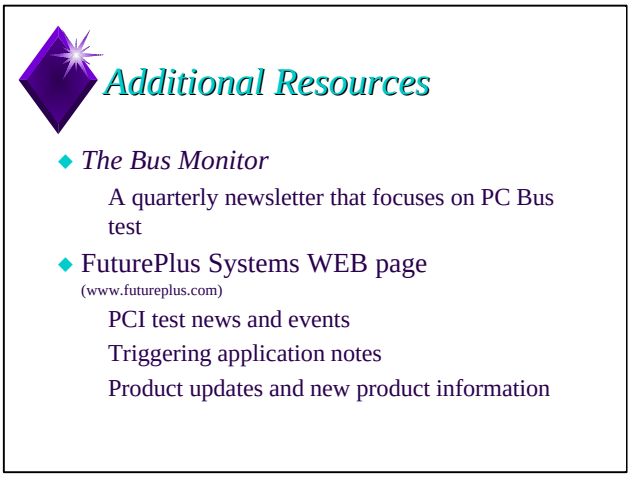
With the deep memory options available on PCI tools, post processing filters make it easy to remove all but the transactions of interest. Also the address mapping of common I/O and memory addresses help navigate through megabytes of acquired PCI traffic.



Which PCI are you doing? FuturePlus and Hewlett-Packard have teamed up to offer the broadest PCI tool offering in the industry.



Embedded PCI? No problem we can show you how.
Do you think PCI-X is in your future? Give us a call…it's in our future too!



For more information about the tools mentioned in this presentation please contact: your nearest Hewlett-Packard sales office or

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